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# Multilevel Cascaded Inverters under Unbalanced DC Sources

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**Abstract—***This paper proposes a pulse width - modulation strategy to achieve balanced line-to-line output voltages and to maximize the modulation index in the linear modulation range where the output voltage can be linearly adjusted in the multilevel cascaded inverter operating under unbalanced dc-link conditions.*

**Keywords:** *Harmonic injection, multilevel cascaded inverter, neutral voltage modulation, phase-shifted modulation, space vector pulse width modulation.*

## 1. INTRODUCTION

MULTILEVEL inverter enables the synthesis of a sinusoidal output voltage from several steps of voltages. For this reason, multilevel inverters have low *dv/dt* characteristics and generally have low harmonics in the output voltage and current. In addition, switching of very high voltages can be achieved by stacking multilevel inverter modules

Due to these advantages, multilevel inverters have been applied in various application fields. Among various topologies for multilevel inverter, the multilevel inverters of its simple structure is one of the prominent topologies because for modularization.

In various application fields , Among various topologies for multilevel inverters, the multilevel cascaded inverter (MLCI) structure is one of the prominent topologies because of its simple structure for modularization and fault-tolerant capability. Therefore, MLCIs are used for many applications, such as dynamic voltage restorer, static synchronous compensator(STATCOM), high-voltage energy storage device, photovoltaic inverters, medium-voltage drives, electric vehicle (EV) traction drives, and so on. In MLCI applications, a modulation strategy to generate gating signals is very crucial to achieve high-performance control. Regarding this issue, many studies have been conducted, and they are roughly categorized into multilevel selective harmonic elimination pulsewidth modulation (PWM) (SHEPWM), multilevel carrier-based PWM, and multilevel space vector PWM (SVPWM) methods .Generally, a carrier-based PWM or SVPWM is preferred in applications such as motor drives , where dynamic properties are very important, whereas SHEPWM is preferred in some high-power static power conversion applications. In, an SVPWM method has been studied to cover over modulation range in the multilevel inverter.

In , an SVPWM method has been studied to coverthe over modulation range in the multilevel inverter. To reduce the common-mode voltage, a multilevel SVPWM has been proposed in . The series SVPWM method has been reported to easily implement SVPWM for the MLCI .In , an SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. As with two-level inverters, it is also possible to implement carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the three-phase references .In some methods to calculate the offset voltages to achieve the optimal space vector switching sequence are addressed.

The performances of a carrier-based PWM and an SVPWM are compared, and a PWMscheme is proposed to obtain an optimal output voltage in the multilevel inverter a zero sequencecomponent helps to obtain the maximum balanced output voltages in a fault condition. In , an offset voltage injection technique is studied to balance the output voltage of the MLCI, but the use of an integrator in the compensation method may reduce dynamic characteristics in applications such as EV motor drives. Recently, the multilevel multiphase feed forward space vector modulation technique called MFFSVM is proposed to compensate the this paper, a carrier-based PWM strategy to balance line-to- line output voltages and to maximize the linear modulation range where the output voltage can be linearly controlled in the MLCI operating under unbalanced dc-link conditions is proposed. In unbalanced dc-link conditions, the maximum synthesizable voltage in each phase is not uniform. the maximum linear modulation range consideringunbalanced dc sources is evaluated. After that, a neutral voltage modulation (NVM) strategy is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in

theory. In the proposed method, the neutral voltage reference, which considers a zero sequence voltage to compensate the output voltage imbalance, and an offset voltage to extend the linear modulation range areeasily obtained through simple arithmetic calculations imbalances in MLCI

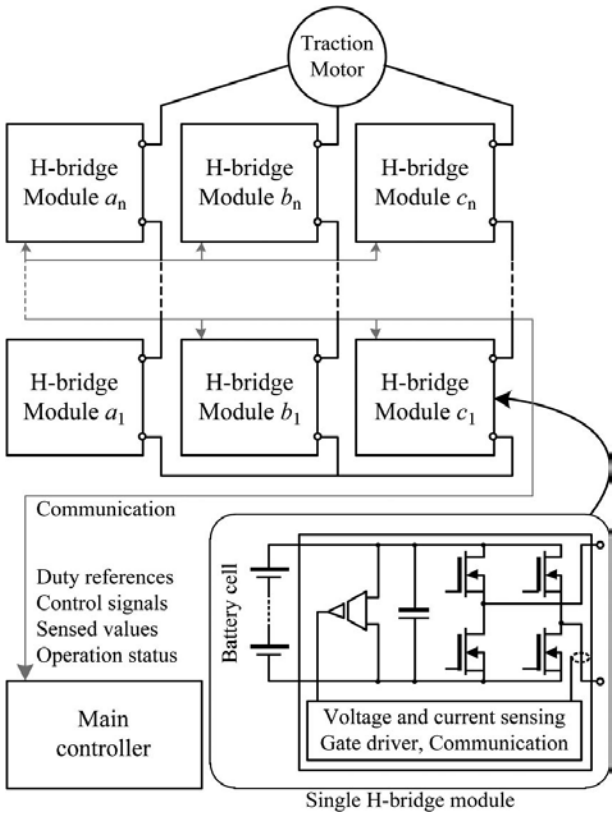



**Fig. 1: MLCI-based inverter for EV traction drive.**

## 2. SYSTEM CONFIGURATION AND VOLTAGE VECTOR SPACE ANALYSIS

### 2.1 Configuration of MLCI for EV Traction Motor Drive

Fig. 1 shows the EV traction motor drive system that is dealt with in this paper. In this configuration, various power ratings can be easily implemented by configuring the number of the single H-bridge modules according to a required specification such as a neighborhood EV, full-size sedan, and so on. Here, each H-bridge module incorporates voltage and current sensing circuitries, gate drivers, and communication interfaces between the module itself and the main controller. In addition, batterycells can be also included in the H-bridge module. The unipolar modulation technique is applied between two switching legs in the H-bridge module. Consequently, the effective switching frequency in each H-bridge module is twice the carrier frequency.

In addition to this, the well-known PS modulation technique is used to implement interleaving and multilevel operation Therefore, the effective switching frequency $f_{sw}$in a phase is

$$fsw = 2N \times fc \quad (1)$$

where$N$ and $f_c$ represent the number of the H-bridge modules in each phase and the carrier frequency of PWM, respectively. As an example, Fig. 2 shows the carriers for each module, the duty cycles in unipolar modulation, and the output voltage when $N = 2$.

### 2.2 Voltage Vector Space Analysis

When the dc-link voltage of a single H-bridge module is $V_{dc}$, the out put voltage $v_{pn}$has three states, i.e., $V_{dc}$, 0, and $-V_{dc}$,

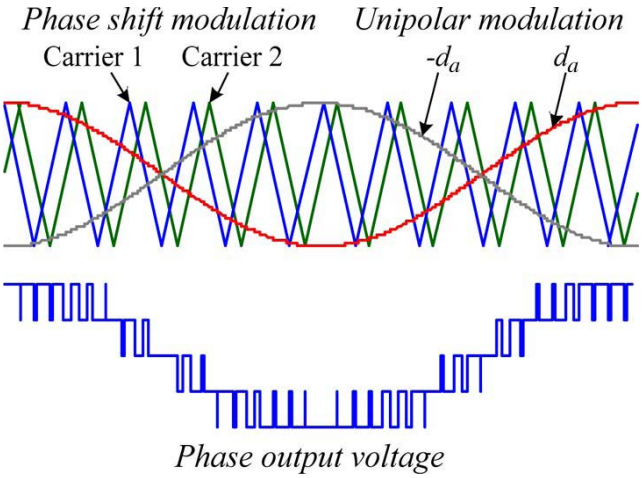



**Fig. 2**

By adopting the concept of a switching function, it can be represented as

vpn=SpVdc

Sp ∈{−1, 0, 1}p=a,b,or,c(2)

where$S_p$ is a switching function and $p$ can be replaced with $a$, $b$, or $c$, which represent the phases.

## 3. PROPOSED MODULATION TECHNIQUE

In Section II, the maximum synthesizable voltage in thelinear modulation range was evaluated under the unbalanced dc links. In this section, a method is proposed to realize the maximum modulation index in the linear modulation range under these conditions.

### 3.1 Traditional Offset Voltage Injection Method

The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory behind this is that an offset voltage is incorporated with phase voltage references to implement various PWMschemes in carrier-basedPWM by using the fact that line-to-line voltages are applied to a three-phase load . For example, the offset voltage$v*sn$is injected to the phase voltage references $v*as$, $v*bs$, and $v*cs$to implement carrier-based SVPWM as in

$v*sn=v*\max+ v*\min$

2

$v*\max = \max(v*as, v*bs, v*cs)$

$v*\min = \min(v*as, v*bs, v*cs).$ (3)

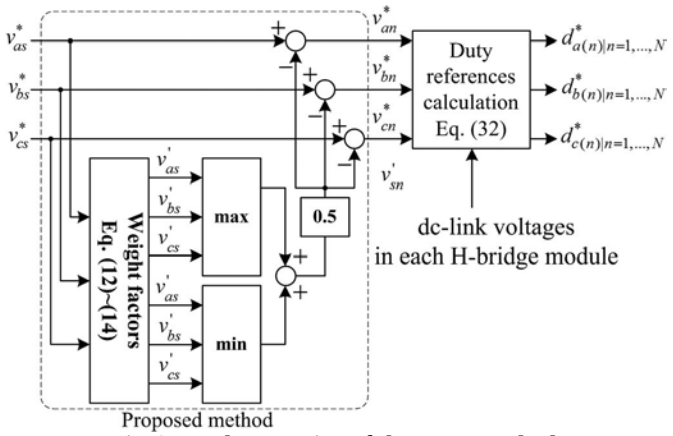



**Fig. 3: Implementation of the NVM method**

### 3.2 Proposed NVM Method

If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage reference approaches $V_{ph\_max}$. This is because the traditional methods are not considering unbalanced dc-link conditions. Therefore, even if a phase can synthesize an output voltage.

Reference in the linear modulation range, the other phases can be saturated or go into the over modulation region. In this situation, a neutral voltage can be produced by the saturated or over modulated phase. In order to resolve this issue and to synthesize the output voltage to $V_{ph_max}$in the linear modulation range, the NVM technique is proposed in this paper.The concept of the proposed NVM technique. Here, a neutral voltage between the two neutral points *n* and *s* is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant *Kw*is defined as

By using (4), the weight factors are calculated a

Kw_a= Kw
Vdc_a
Kw_b= Kw
Vdc_b
Kw_c= Kw
Vdc_c (4)

v_as=Kw_av*asv_bs=Kw_bv*sv_cs=Kw_cv*cs. (5)

Matlab simulation. The three-phase *RL* load with $R$ = 0.1Ωand$L$ = 1mH is employed. The dc-link voltages for each phase are$V_{dc_a}$= 0.5 × 30 V, $V_{dc\_b}$= 0.75 × 30 V $V_{dc\_c}$

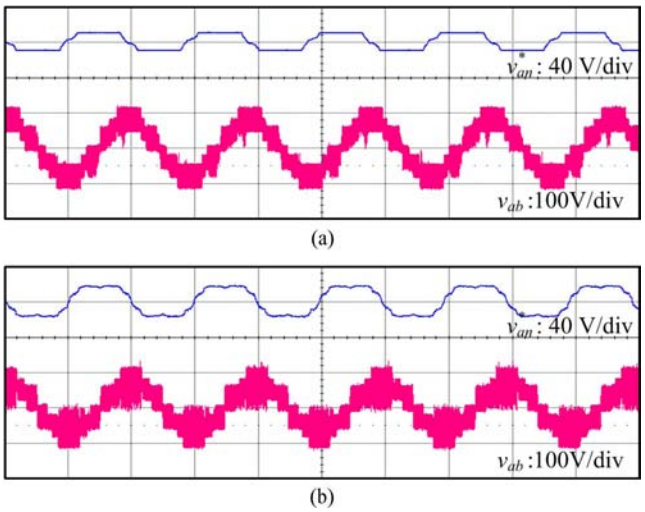



**Fig. 4: a) Traditional SVPWM**

Fig. Experimental result of the traditional SVPWM and the proposed NVM Strategies.

## 4. OVERVIEW

As with two-level inverters, it is also possible inverter operating under unbalanced dc-link conditions, the maximumsynthesizable voltage in eachphase isnot uniform. Consequently, the linear modulation range is reduced and a significant output voltage imbalance may occur as output voltage references increases. In order to analyze the imbalance effect, the voltage vector space for the multilevel cascaded inverter is evaluated in detail.

In the MATLAB, Simulink using Simpower systems tool box and to verify the results through various case studies applying maximum linear modulation range considering unbalanced dc sources is evaluated. These are generally complex and difficult to detect when a Unbalanced Load voltages. That is the ideal DC line supply should be a pure sine wave.

## 5. RESEARCH PROBLEM

The aim of the project is to implement, a carrier-based PWM strategy to balance line-to-line output voltages and to maximize the linear modulation range where the output voltage can be linearly controlled in multilevel cascaded inverter operating under unbalanced dc-link conditions, the maximumsynthesizable voltage in eachphase isnot uniform. Consequently, the linear modulation range is reduced and a significant output voltage imbalance may occur as output voltage references increases. In order to analyze the imbalance effect, the voltage vector space for the multilevel cascaded inverter is evaluated in detail.

In the MATLAB, Simulink using Simpower systems tool box and to verify the results through various case studies applying maximum linear modulation range considering unbalanced dc sources is evaluated.

The carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the three-phase references.

## 6. LITERATURE REVIEW

J. Rodriguez, J.-S. Lai, and F. Z. Peng, Proposed "Multilevel inverters: A survey of topologies, controls, and applications Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate DC sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulsewidth modulation, multilevel selective harmonic elimination, and space-vector modulation. Special attention is dedicated to the latest and more relevant applications of these converters such as laminators, conveyor belts, and unified power-flow controllers. The need of an active front end at the input side for those inverters supplying regenerative loads is also discussed, and the circuit topology options are also presented. Finally, the peripherally developing areas such as high-voltage high-power devices and optical sensors and other opportunities for future development are addressed.

M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, Proposed "A survey on cascaded multilevel inverters," Cascaded multilevel inverters synthesize a medium-voltage output based on a series connection of power cells which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. Due to these features, the cascaded multilevel inverter has been recognized as an important alternative in the medium-voltage inverter market. This paper presents a survey of different topologies, control strategies and modulation techniques used by these inverters. Regenerative and advanced topologies are also discussed. Applications where the mentioned features play a key role are shown. Finally, future Develop

## 7. PHOTOGRAPHY OF THE SETUP

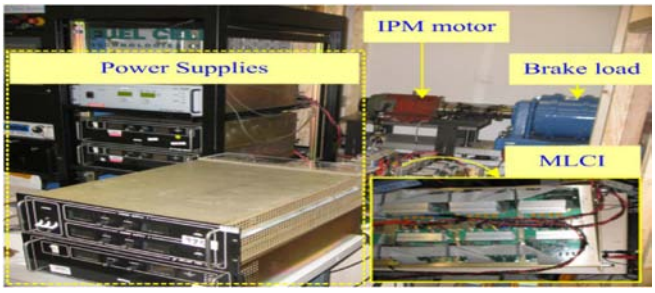
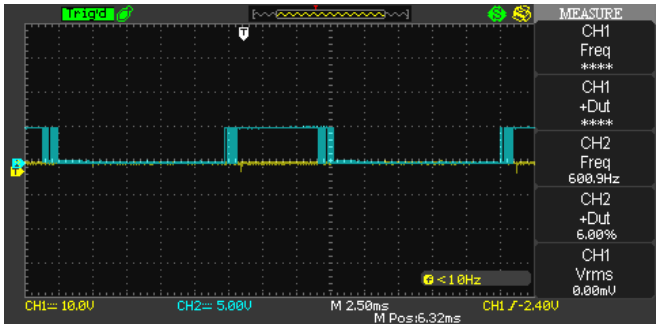
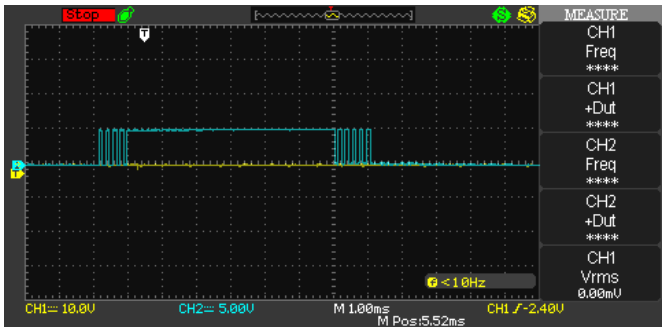



**Fig. 5: Photography of the experimental setup**

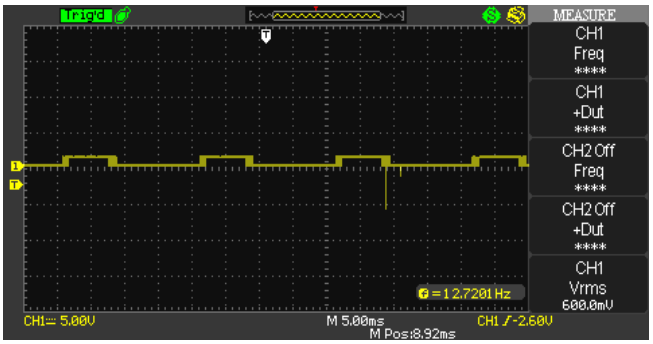
## 8. EXPECTED WAVEFORMS



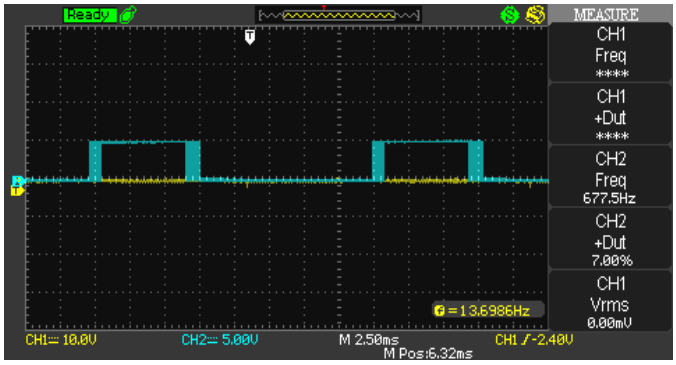

a) Controller output



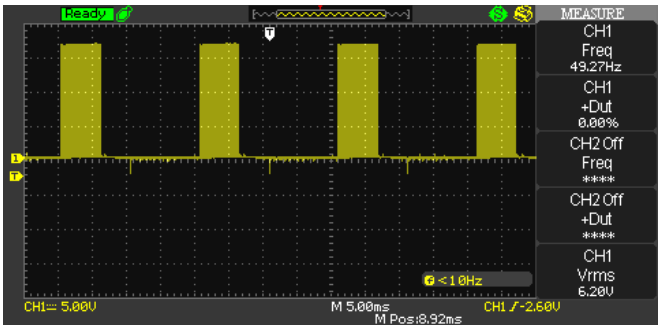

b) Chopping circuit output



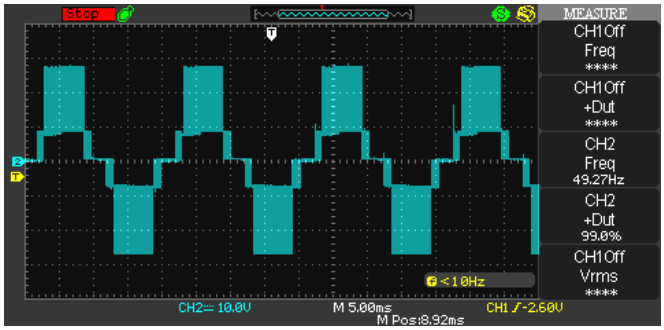

c) Optocoupler input




d) Optocoupler output




e) Transistor output




f) Final output

## 9. CLOSED LOOP CIRCUIT FOR MULTILEVE CASCADED INVERTER

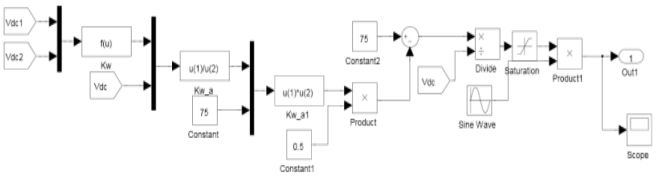



**Fig. 6: Closed loop circuit diagram**

## 10. SIMULATION CIRCUIT FOR MULTILEVEL CASCADED INVERTER UNDER UNBALANCED DC SOURCE

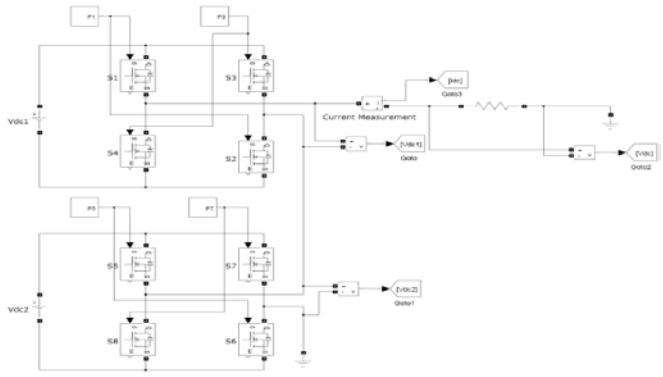
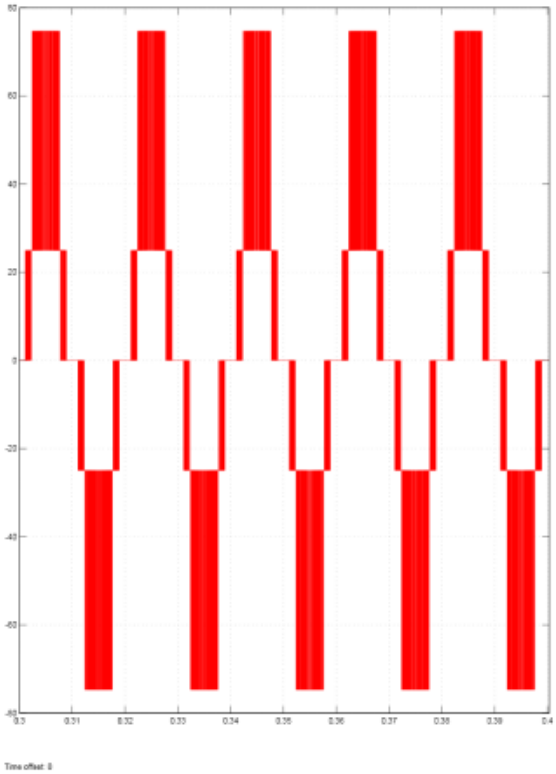
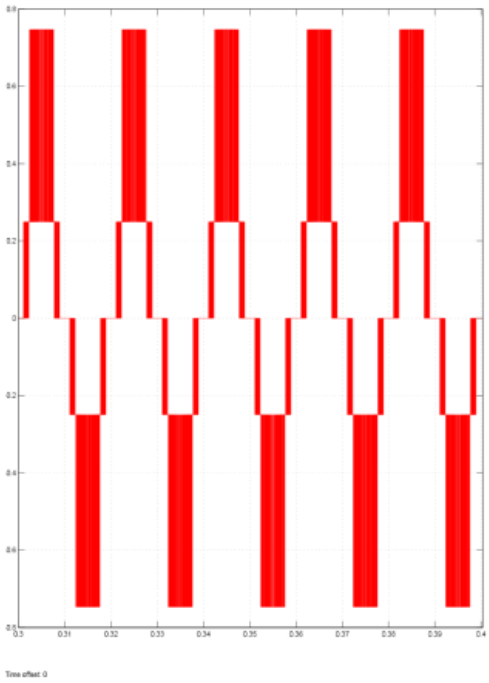



**Fig. 7: Simulation Circuit Diagram**

## 11. SIMULATION EXPECTED WAVEFORMS



a) Level Voltage waveforms



b) Level Current waveforms

## 12. ADVANTAGES AND CONCLUSION

### ADVANTAGES

The multilevel cascaded inverter uses full H-bridge connected is series to produce inverter AC from separate DC source. These DC sources. These DC sources can be any natural resource such as sunlight or wind energy or anything.

- It does not need any capacitors or diodes for clamping
- The wave is quite sinusoidal in nature even if you don't filter it.

## 13. CONCLUSION

The NVM technique for MLCIs under unbalanced dc-link conditions has been proposed in this paper. In order to analyze the maximum synthesizable voltage of MLCIs, the voltage vector space has been analyzed using the switching function. From the analysis, the maximum linear modulation range was derived. The proposed NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. Both simulations and experimental results based on the IPM motor drive application verify the effectiveness of the proposed method.

### REFERENCES

[1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[3] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed ofpower converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[4] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey